Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (currently amended) A semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising:

a first semiconductor chip which includes a plurality of first bonding pads outputting first signals having a first level; and

a second semiconductor chip which includes

a plurality of second bonding pads electrically coupled to a part of the plurality of first bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of first bonding pads,

a plurality of third bonding pads, and

a signal level conversion circuit configured to convert the first signals of the first level into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads, and

wherein said first level and said second level correspond to respective, different driving voltages in a digital circuit, and

wherein the second semiconductor chip includes one or more digital circuits configured to receive and operate with signals of the first level as well as signals of a second level corresponding to a second driving voltage.

2. (original) The semiconductor device as defined in Claim 1, wherein the second level is greater than the first level.

Claims 3-9 (canceled).

10. (currently amended) A semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising:

a first semiconductor chip which outputs one or more first signals having a first level; and

a second semiconductor chip which includes a signal level conversion circuit,

wherein said signal level conversion circuit converts the first signals of the first level from the first semiconductor chip into second signals having a second level different from the first level, [[and]]

wherein said first level and said second level correspond to respective, different first and second driving voltages in a digital circuit, and

wherein the second semiconductor chip includes one or more digital circuits configured to receive and operate with signals of the first level as well as signals of a second level corresponding to a second driving voltage.

11. (previously presented) The semiconductor device as defined in Claim 10, wherein said signal level conversion circuit includes a buffer driven at the second level.

12. (previously presented) The semiconductor device as defined in Claim 11, wherein said

buffer converts an input signal at the first level into an output signal at the second level.

13. (previously presented) The semiconductor device as defined in Claim 10, wherein said signal level conversion circuit includes an I/O interface circuit adapted for bi-directional data flow.

14. (previously presented) The semiconductor device as defined in Claim 13, wherein said I/O interface circuit includes one or more tri-state circuits.

15. (previously presented) The semiconductor device as defined in Claim 10, wherein the second level is greater than the first level.

16. (previously presented) A digital system including the semiconductor device as defined in Claim 10, and a second semiconductor device, wherein said second semiconductor device is driven by a driving voltage corresponding to said second level, and said second signals from said semiconductor device as defined in Claim 10 are input by said second semiconductor device.

17. (previously presented) [[The]] A semiconductor device ~~of Claim 1~~ which integrates a plurality of semiconductor chips into a single package, comprising:

a first semiconductor chip which includes a plurality of first bonding pads outputting first signals having a first level; and

a second semiconductor chip which includes

a plurality of second bonding pads electrically coupled to a part of the plurality of first

bonding pads to receive the first signals having the first level from the first semiconductor chip through the part of the plurality of first bonding pads,

a plurality of third bonding pads, and

a signal level conversion circuit configured to convert the first signals of the first level into second signals having a second level different from the first level and outputs the second signals through the plurality of third bonding pads, and

wherein said first level and said second level correspond to respective, different driving voltages in a digital circuit, and

wherein said second semiconductor chip includes one or more digital circuits which are tolerant both to digital input signals of the first level and to digital input signals of the second signal level.

Claim 18 (canceled).